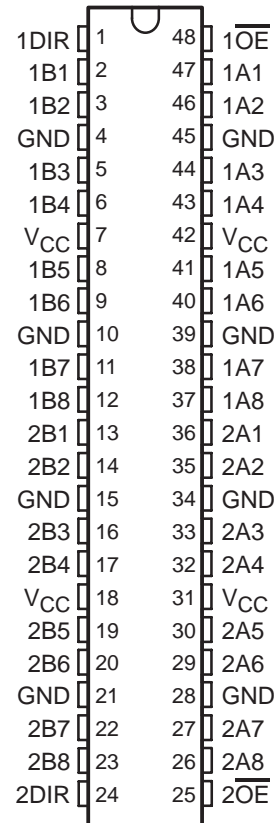


SN74LVTH162245-EP 3.3-V ABT 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG OR DL PACKAGE
(TOP VIEW)



† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74LVTH162245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses effectively are isolated.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description/ordering information (continued)

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

ORDERING INFORMATION

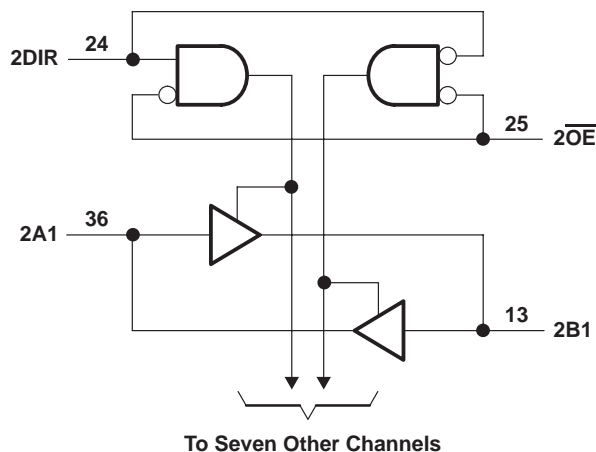
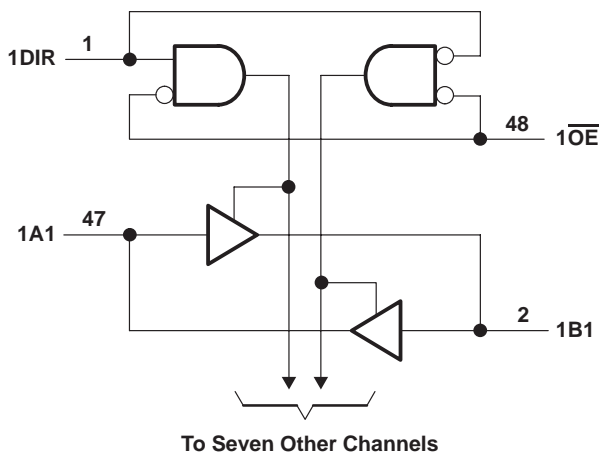
TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	CLVTH162245IDGGREP	LH162245EP
-55°C to 125°C	SSOP – DL	Tape and reel	CLVTH162245MDLREP	LVTH162245EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : B port	128 mA
A port	30 mA
Current into any output in the high state, I_O (see Note 2): B port	64 mA
A port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DL package	95°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

recommended operating conditions (see Note 5)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage		5.5	V
I_{OH}	High-level output current	A port	–12	mA
		B port	–32	
I_{OL}	Low-level output current	A port	12	mA
		B port	64	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		μ s/V
T_A	Operating free-air temperature	SN74LVTH162245I	–40	85
		SN74LVTH162245M	–55	125

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA				-1.2	V
V _{OH}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} - 0.2			V
		V _{CC} = 3 V, I _{OH} = -12 mA		2			
	B port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} - 0.2			
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4			
		V _{CC} = 3 V, I _{OH} = -32 mA		2			
V _{OL}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OL} = 100 μA				0.2	V
		V _{CC} = 3 V, I _{OL} = 12 mA				0.8	
	B port	V _{CC} = 2.7 V, I _{OL} = 100 μA				0.2	
		I _{OL} = 24 mA				0.5	
		V _{CC} = 3 V, I _{OL} = 16 mA				0.4	
		I _{OL} = 32 mA				0.5	
		I _{OL} = 64 mA				0.55	
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND				±1	μA
		V _{CC} = 0 V or 3.6 V, V _I = 5.5 V				10	
	A or B port‡	V _{CC} = 3.6 V, V _I = 5.5 V				20	
		V _I = V _{CC}				5	
		V _I = 0				-10	
I _{off}	V _{CC} = 0 V, V _I or V _O = 0 to 4.5 V				±100	μA	
I _{I(hold)}	A or B port	V _{CC} = 3 V, V _I = 0.8 V		75			μA
		V _I = 2 V		-75			
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V		500		-750	
I _{OZPU}	V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA	
I _{OZPD}	V _{CC} = 1.5 V to 0 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care				±100	μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0 V, V _I = V _{CC} or GND		Outputs high		0.19		mA
			Outputs low		5		
			Outputs disabled		0.19		
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		SN74LVTH162245I		0.2		mA
			SN74LVTH162245M		0.3		
C _i	V _I = 3 V or 0 V				4	pF	
C _{io}	V _O = 3 V or 0 V				10	pF	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused pins at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

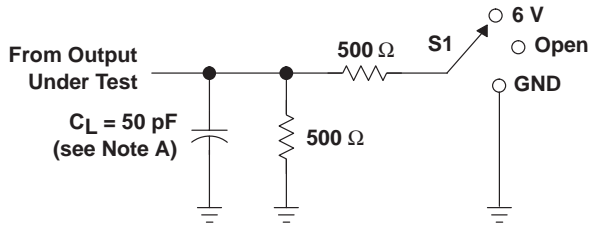
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVTH162245I				SN74LVTH162245M				UNIT	
			$V_{CC} = 3.3$ V ± 0.3 V			$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 2.7$ V		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN		MAX
t _{PLH}	A	B	1	2.3	3.3	3.7		1	3.5	4		ns
t _{PHL}			1	2.2	3.3	3.5		1	3.5	3.9		
t _{PLH}	B	A	1	2.8	4	4.6		1	4.3	5.3		ns
t _{PHL}			1	2.5	3.4	3.6		1	4.2	4.5		
t _{PZH}	\overline{OE}	B	1	2.8	4.6	5.4		1	4.8	5.9		ns
t _{PZL}			1	3	4.6	5.2		1	4.8	5.5		
t _{PZH}	\overline{OE}	A	1	3.3	5.3	6.3		1	5.5	7.2		ns
t _{PZL}			1	3.3	5.1	5.8		1	7.2	6.4		
t _{PHZ}	\overline{OE}	B	1.5	3.8	5.2	5.5		1.5	6.4	5.8		ns
t _{PLZ}			1.5	3.5	5.1	5.4		1.5	5.8	5.8		
t _{PHZ}	\overline{OE}	A	1.5	4	5.6	5.9		1.5	5.8	6.5		ns
t _{PLZ}			1.5	3.8	5.5	5.5		1.2	6.3	6.3		
t _{sk(o)}					0.5						ns	

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

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3.3-V ABT 16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

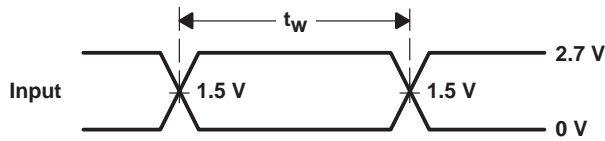
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PARAMETER MEASUREMENT INFORMATION

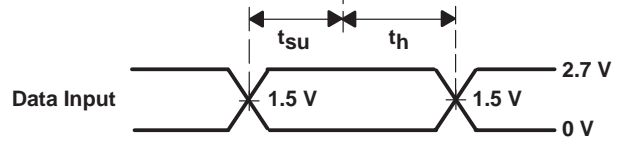


LOAD CIRCUIT

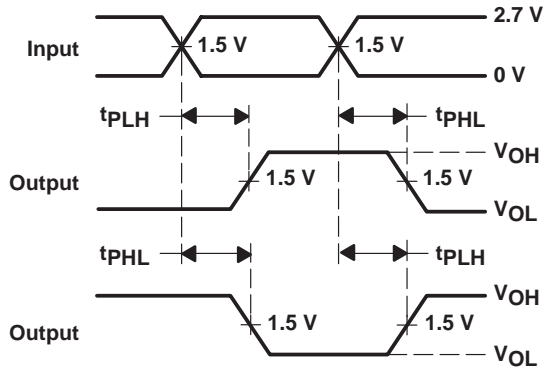
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



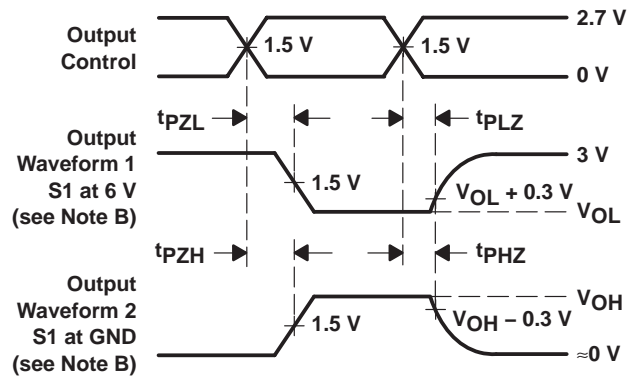
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CLVTH162245IDGGREP	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CLVTH162245MDLREP	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04709-01XE	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04709-02YE	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74LVTH162245](#)
- Military: [SN54LVTH162245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVTH162245IDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CLVTH162245MDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVTH162245IDGGREP	TSSOP	DGG	48	2000	346.0	346.0	41.0
CLVTH162245MDLREP	SSOP	DL	48	1000	346.0	346.0	49.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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